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Richard J. Cloutier, Donald E. Thomas

July 1993 **Proceedings of the 30th international conference on Design automation**

Full text available: [pdf\(796.47 KB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

2 [Automatic Verification of In-Order Execution In Microprocessors with Fragmented Pipelines and Multicycle Functional Units](#)

P. Mishra, N. Dutt, A. Nicolau, H. Tomiyama

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: [pdf\(163.99 KB\)](#)

Additional Information: [full citation](#), [abstract](#)

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As embedded systems continue to face increasingly higherperformance requirements, deeply pipelined processor architectures are being employed to meet desired system performance. System architects critically need modeling techniques that allow exploration, evaluation, customization and validation of different processor pipeline configurations, tuned for a specific application domain. We propose a novel Finite State Machine (FSM) based modeling of pipelined processors and define a set of properties th ...

3 [Instruction issue logic for high-performance, interruptable pipelined processors](#)

G. S. Sohi, S. Vajapeyam

June 1987 **Proceedings of the 14th annual international symposium on Computer architecture**

Full text available: [pdf\(814.60 KB\)](#)

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4

[Code size reduction technique and implementation for software-pipelined DSP](#)

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